Claims

We claim:

1. A resynchronization process for use in a data communication system having a first device configured to transmit data at a symbol rate to a second device, the second device including a Reed Solomon (RS) decoder having a RS lock indicator and a Moving Picture Experts Group (MPEG) Protocol Interface (MPI) having a MPI lock indicator, the method comprising the steps of:

(a) detecting whether the RS lock indicator is locked;

(b) detecting whether the MPI lock indicator is locked;

(c) ending the resynchronization process, when in a first state where the RS lock indicator is locked and the MPI indicator is locked, indicating that synchronization exists;

(d) performing a channel acquisition algorithm in accordance with the data communication system, when the system is in a second state where the RS lock indicator is unlocked and the MPI indicator is locked;

(e) monitoring the RS lock indicator and the MPI lock indicator during a first predetermined time interval when the system is in the third state where the RS lock indicator is unlocked and the MPI indicator is locked, waiting for synchronization to occur in the RS decoder and the MPI hardware block,

(i) wherein, during the third state, the resynchronization process ends when the MPI indicator switches to locked and the monitoring time is less than or equal to the first predetermined time interval, indicating that synchronization exists,

(ii) wherein an intermediate-subset of the channel acquisition algorithm is performed and the resynchronization process ends, when in the third state, the RS lock indicator switches to unlocked and the monitoring time is less than or equal to the first predetermined time interval, and

(iii) wherein a channel acquisition algorithm is performed, when in the third state, the monitoring time is greater than the first predetermined time interval and synchronization does not exist; and

(f) performing the intermediate-subset of the channel acquisition algorithm during a second predetermined time interval when the system is in the fourth state where the RS lock indicator is unlocked and the MPI indicator is unlocked,

(i) wherein the RS lock indicator and the MPI lock indicator are monitored, awaiting synchronization to occur in the RS decoder and the MPI hardware block,

(ii) wherein, in the fourth state, the resynchronization process ends when both the RS lock indicator and the MPI indicator switch to locked, indicating synchronization exists, and

(iii) wherein the channel acquisition algorithm is performed, when in the fourth state, the monitoring time is greater than the second predetermined time interval and synchronization does not exist.

2. The resynchronization process as recited in Claim 1, wherein the intermediate-subset of the channel acquisition algorithm includes the steps of:

(i) determining the burst boundaries,

(ii) performing channel acquisition, if the burst size fails,

(iii) applying fractional frequency correction,

(iv) applying integer frequency correction until the integer frequency offset is zero,

(v) waiting for a voltage-controlled crystal oscillator (VCXO) within the data communication system to settle,

(vi) determining if the integer frequency offset is zero,

(vii) determining if the fractional frequency offset is below a first threshold,

(viii) repeating steps iii – vii if the time spent performing frequency correction and acquisition is less than a predetermined frequency lock loop time and the integer frequency offset is not equal to zero or the fractional frequency offset is not below a first threshold,

(ix) performing Cyclic Prefix Sequence (CPS) demodulation to obtain a proper sequence of training tone phase sets if the integer frequency offset is equal to zero and the fractional frequency offset is below a first threshold,

(x) performing channel acquisition, if the time spent performing frequency correction and acquisition is equal to or greater than the predetermined frequency lock loop time and the integer frequency offset is not equal to zero or the fractional frequency offset is not below a first threshold,

(xi) performing Forward Error Correction (FEC) initialization,

(xii) clearing a plurality of First-In First-Out registers associated with the data communication system,

(xiii) detecting whether the RS lock indicator is locked,

(xiv) determining if the time spent securing a RS lock is less than a predetermined RS lock time,

(xv) repeating steps i - xiv if the time spent securing a RS lock is less than a predetermined RS lock time,

(xvi) determining if the time spent securing a MPI lock is less than a predetermined MPI lock time,

(xvii) repeating steps i - xvi if the time spent securing a MPI lock is less than a predetermined MPI lock time,

(xviii) determining if the time in the resynchronization process is less than a second predetermined time,

(xix) repeating steps i - xviii if the time in the resynchronization process is less than a second predetermined time.

3. A wireless access modem coupled to receive an incoming analog signal, the wireless access modem comprises:

an analog-to-digital converter (ADC) to convert the incoming analog signal into a digital signal;

a receiver portion coupled to the ADC to receive the converted digital signal;

at least one digital signal processing module defining the Physical (PHY) layer coupled to the receiver portion for processing the digital signal, the at least one digital signal processing module including,

a Reed Solomon (RS) decoder having a RS lock indicator, and

a Moving Picture Experts Group (MPEG) Protocol Interface (MPI) coupled to the RS decoder, the MPI having a MPI lock indicator, wherein resynchronization of the wireless access modem occurs depending upon the value of the RS lock indicator and the MPI lock indicator within the PHY layer;

a medium access control (MAC) layer coupled to the at least one digital signal processing module;

a host interface coupled to the MAC layer to provide an interface between a host and the wireless access modem;

a transmitter portion coupled to the MAC layer; and

a digital-to-analog filter coupled to the transmitter portion for converting the digital signal to an analog signal.

4. A wireless access modem as recited in claim 3, wherein the receiver portion comprises:

a finite impulse response (FIR) filter;

a Fast Fourier transform (FFT) filter coupled to the FIR filter; and

an intermediate frequency (IF) storage unit coupled to receive the FFT signal.

5. A wireless access modem as recited in claim 3, wherein the at least one digital signal processing module comprises:

a noise estimation module coupled to receive the filtered digital signal to estimate the noise in the signal;

a channel estimation module coupled to the noise estimation module to calculate a channel estimation metric;

a first-in first-out (FIFO) filter coupled to receive the filtered digital signal;

a bit deinterleaver coupled to the FIFO filter to bit deinterleave the filtered digital signal;

a unpuncturing module coupled to receive the deinterleaved signal to unpuncture the signal;

a Viterbi decoder coupled to receive the unpunctured signal to decode the signal;

a byte deinterleaver coupled to receive the Viterbi decoded signal to deinterleave the byte;

a descrambler coupled to receive the byte deinterleaved signal to descramble the signal; and

a Reed-Solomon decoder coupled to receive the descrambled signal to decode.

6. A wireless access modem as recited in claim 3, wherein the transmitter portion comprises:

a forward error correction (FEC) module to provide error correction filtering to a received signal;

an Inverse Fast Fourier transform (IFFT) filter coupled to receive the forward error corrected signal; and

a second finite impulse response filter coupled to the IFFT to filter the signal for transmission.